

ABSTRACT

A circuit which accurately controls the word line (pass transistor gate) driving voltage to a voltage which is both controlled and is not significantly greater than is needed to drive the word line. The elements of the present invention eliminate the need for a double-boot-strapping circuit, and ensure that no voltages exceed that necessary to fully turn on a memory cell access transistor. Accordingly, voltages in excess of that which would reduce reliability are avoided, and accurate driving voltages are obtained. A DRAM is comprised of word lines, memory cells having enable inputs connected to the word lines, apparatus for receiving word line selecting signals at first logic levels V_{ss} and V_{dd} , and for providing a select signal at levels V_{ss} and V_{dd} , a high voltage supply source V_{pp} which is higher in voltage than V_{dd} , a circuit for translating the select signals at levels V_{ss} and V_{dd} to levels V_{ss} and V_{pp} and for applying it directly to the word lines for application to the enable inputs whereby an above V_{dd} voltage level word line is achieved without the use of double boot-strap circuits.

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